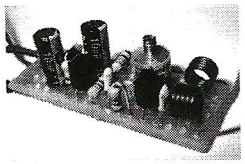
İZMİR UNIVERSITY OF ECONOMICS
Department of Computer Engineering
ETE 232 Microelectronic Devices and Circuits



Spring 2011/2012

MIDTERM #1

April 7, 2012
120 min

SOLUTIONS

INSTRUCTIONS

- Closed book, closed notes.
- Calculators are allowed, but borrowing is not allowed.
- Your mobile phones must be turned off during the exam.
- You must show your work for all problems to receive full credit; simply providing answers will result in only partial credit, even if the answers are correct.
- Put your name on any additional material that you submit.
- Be sure to provide units.
- Please indicate the number of page where your work is to be continued.
- Do not spend all your time on one problem and on one part and attempt to solve all of them.
- Please sign the honor pledge that is provided below.

Honor Pledge: I have neither given nor received any aid on this exam. Signed:……..

Last Name :……

Name :……

Group :……

Student No :……

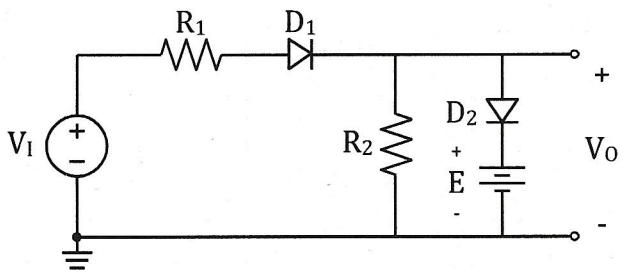
Q	Points	Grade
1	30	
2	30	
3	20	
4	20	
Total	100	

Q1. (30 pts)

(a) (10 pts)Fill in the missing blanks.

i	The region around the p-n juntion containing no mobile electrons or holes is called ***depletion region***.
ii	Electrons in the outermost shell are called **valence** electrons
iii	The valence electrons shared betwen atoms form **a covalent** bond
iv	In order to break the **covalent** bond, the **valence** electron must gain a minimum energy called **bandgap** energy.
v	An **intrinsic** semiconductor is a single crystal semiconductor material with no other types of atoms within the crystal
vi	The lack of an electron in the **covalent** bond is called **a hole**.
vii	Group V elements are called **donor** impurity.
viii	Group III elements are called **acceptor** impurity.
ix	Adding Group III or Group V elements into a semiconductor crystal is called **doping.**
x	A semiconductor that contains Group III atoms is called **p**-type semiconductor.
xi	A semiconductor that contains Group V atoms is called **n**-type semiconductor.
xii	The movement of an electron due to electric field is called **drift**.
xiii	The flow of electrons due to concenration difference is called **diffusion**.
xiv	The velocity of the electrons in an electric field is proportional the electric field intensity. The proportionality constant is called **mobility**.
xv	In an **n**- type semiconductor electrons are majority carriers whereas the **holes** are **minority** carriers.

(10 pts) Consider the diode circuit given on the right with $R_1 = 10\ k\Omega$, $R_2 = 20\ k\Omega$, E = 6 Volts. Assume that the ***diodes*** are ***ideal.***

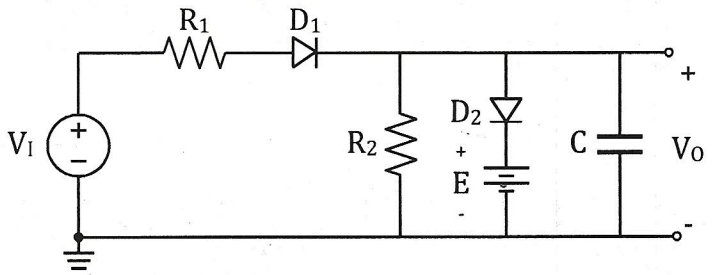


(b) Determine the range of v_s where the diode is ON and the region where the diode is OFF.

(c) Plot the output voltage v_o if

$v_S = 12 \sin 2\pi \cdot 50\ t$ volts

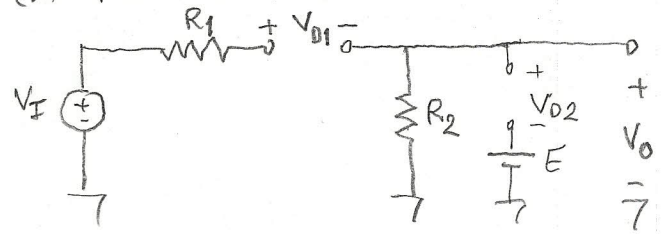
(d) (10 pts) A capacitor C is added to the output of the circuit given in ***part (a).*** Plot the output voltage waveform. Determine the peak and the ripple values.



$v_S = 12 \sin 2\pi \cdot 50\ t$ volts
$R_1 = 10\ k\Omega$,
$R_2 = 20\ k\Omega$.
E = 6 V
C = 10 μF

Solution:

(a) (i) D_1 is OFF ($V_{D1} < 0$) and D_2 is OFF ($V_{D2} < 0$). ($V_o = 0$)



$V_{D1} = V_I - 0 = V_I < 0$

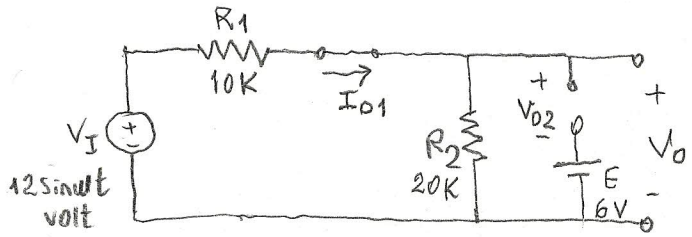
$V_{D2} = -E = -6V < 0$ (Always)

So $V_I < 0 \Rightarrow D_1$ & D_2 are off.

$\Rightarrow V_o = 0$

(Not that if D_1 is OFF, D_2 is also OFF; it cannot be ON.)

ii. D_1 is ON ($I_{D1} \geq 0$); D_2 is OFF ($V_{D2} < 0$) ⇒



$$I_{D1} = \frac{V_I}{R_1+R_2} \geq 0 \Rightarrow V_I \geq 0$$

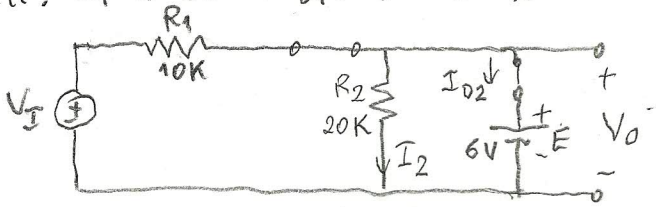
$$V_o = \frac{R_2}{R_1+R_2} \cdot V_I = \frac{2}{3} V_I$$

$$V_{D2} = V_o - E = \frac{2}{3} V_I - 6 < 0 \Rightarrow \frac{2}{3} V_I < 6$$

$$V_I < 9\,V$$

Therefore for $0 \leq V_I < 9V$; D_1 is ON & D_2 is OFF and $V_o = \frac{2}{3} V_I$

iii. D_1 is ON ($I_{D1} \geq 0$) and D_2 is ON ($I_{D2} \geq 0$) ⇒ $V_o = E = 6V$



$$I_{D1} = \frac{V_I - 6}{R_1} = \frac{V_I - 6}{R_1}$$

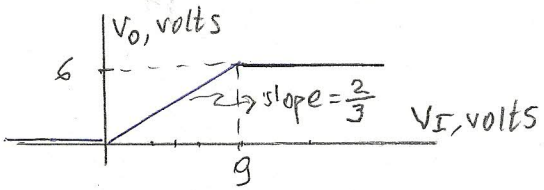
$$I_{D2} = I_{D1} - \frac{E}{R_2} = \frac{V_I - 6}{R_1} - \frac{6}{R_2}$$

$$= \frac{V_I}{R_1} - 6\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = \frac{V_I}{R_1} - 6\,\frac{R_1+R_2}{R_1 R_2}$$

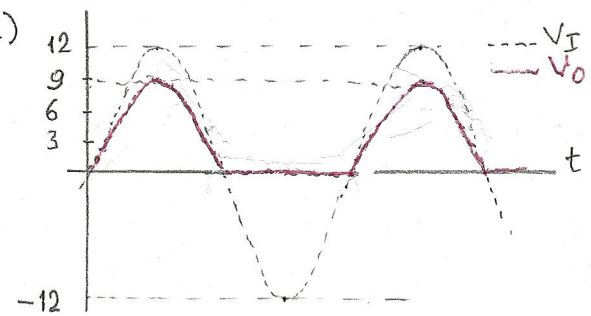
$$I_{D2} > 0 \Rightarrow V_I > 6 \cdot \frac{R_1+R_2}{R_2} = 6 \cdot \frac{30}{20} = 9\,V$$

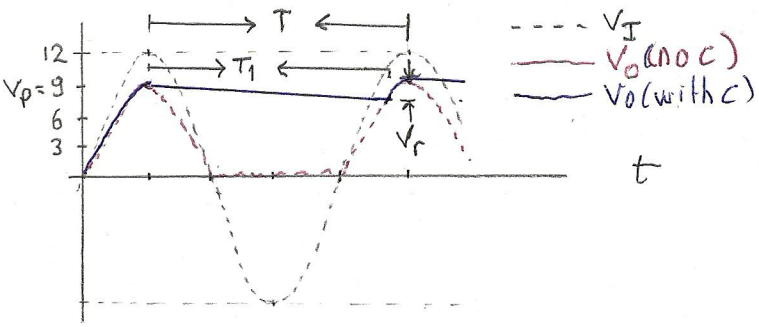
Therefore

$$V_o = \begin{cases} 0 & V_I < 0 \\ \frac{2}{3} V_I & 0 \leq V_I < 9V \\ 6V & 9V \leq V_I \end{cases}$$



(c)





During T_1, C is discharged through R_2 (D is OFF).

$V_p = 9V$

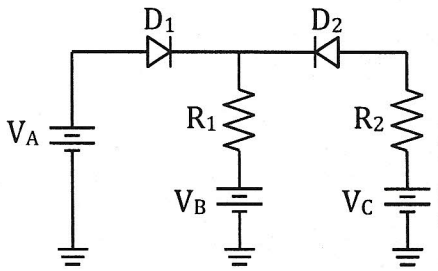
$T_1 \cong T = \frac{1}{f} = \frac{1}{50} = 0.02$ sec. (Discharge period)

$$V_r = \frac{T_1}{R_2 C} \cdot V_p = \frac{0.02}{20\times10^3 \times 10\times10^{-6}} \cdot (9\,V) = \frac{0.02}{0.2} \cdot (9V) = 0.9\,V$$

Q2. (30 pts) Consider the following diode circuits.

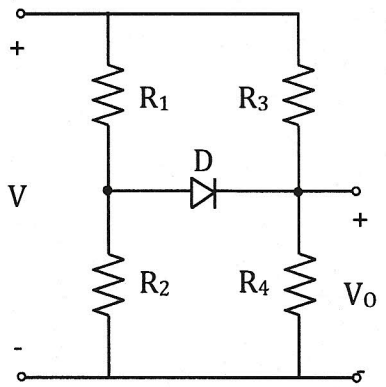
(a) (10 pts) Assuming all diodes are ideal, **determine** and **verify** the states of the diodes, if

V_A= 6 volts
V_B= 4 volts
V_C= 8 volts
R_1= 2 kΩ
R_2= 2 kΩ



(b) (10 pts) Assuming all diodes are ideal, **determine** and **verify** the state of the diode and the output voltage V_O, if

R_1= 6 kΩ
R_2= 3 kΩ
R_3= 3 kΩ
R_4= 3 kΩ
V = 12 volts



(c) (10 pts) Consider the two stage logic gate given on the right.

- For all diodes, the turn-on voltages Vγ = 0.6 volts.
- The input voltages corresponding to the logic levels at V_A, V_B, and V_C are specified as: "Logic 0" = 0 volts; "Logic 1" = 5 volts

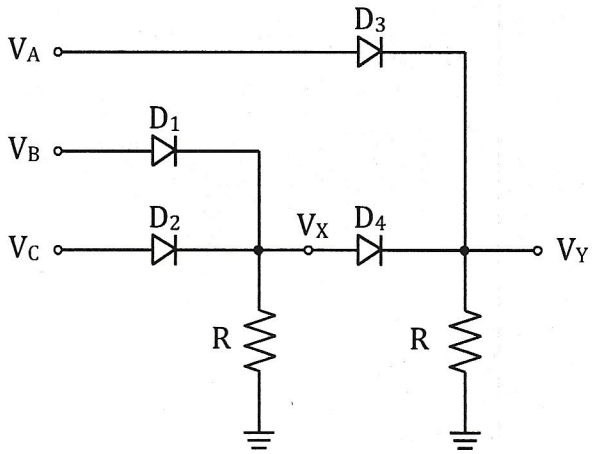
Obtain

- **Voltage Truth Table**

and

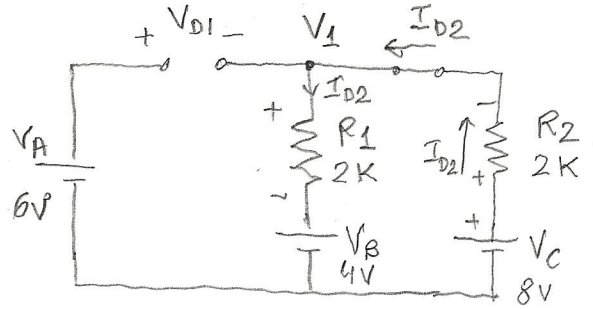
- **Logic Truth Table**

for logic gate given for the outputs **X** and **Y** in terms of the inputs **A, B, C.**



Q2.

(a)



D_1 is OFF (Check : $V_{D1} \leq 0$)

D_2 is ON (Check : $I_{D2} > 0$)

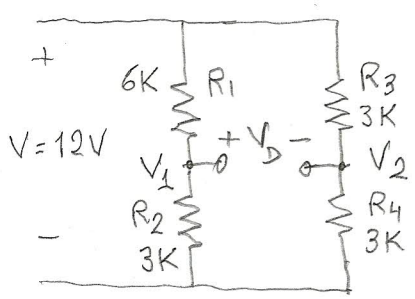
$$I_{D2} = \frac{V_C - V_B}{R_1 + R_2} = \frac{8-4V}{2+2K} = 1mA > 0 \checkmark$$

$$V_1 = R_1 I_{D2} + V_B = (2K)(1mA) + 4V$$
$$= 6V$$

$$V_{D1} = V_A - V_1 = 6 - 6 = 0V \checkmark$$

(D_2 is just at orijin : $I_{D1} = 0$ and $V_{D2} = 0$)

(b)



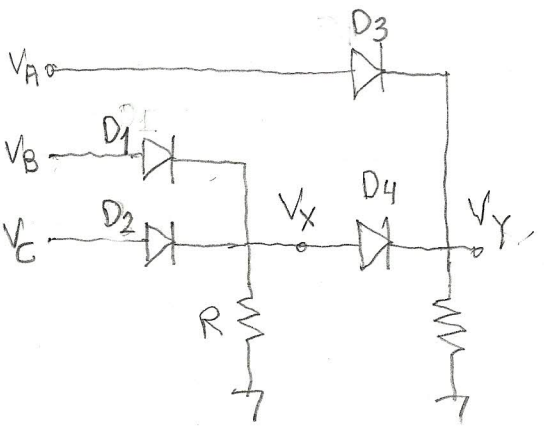
D is off (Check $V_D \leq 0$)

$$V_1 = \frac{R_2}{R_1+R_2} V = \frac{3}{3+6} \cdot 12 = \frac{3}{9} \cdot 12 = 4V$$

$$V_2 = \frac{R_4}{R_3+R_4} V = \frac{3}{3+3} \cdot 12 = \frac{3}{6} \cdot 12 = 6V$$

$$V_D = V_1 - V_2 = 4 - 6 = -2V < 0 \checkmark$$

(c)



Logic Levels : 0V & 5V

Diode turn on : 0.6V

V_A	V_B	V_C	D_1	D_2	V_X	D_3	D_4	V_Y
0	0	0	OFF	OFF	0	OFF	OFF	0
0	0	5	OFF	ON	4.4	OFF	ON	3.8
0	5	0	ON	OFF	4.4	OFF	ON	3.8
0	5	5	ON	ON	4.4	OFF	ON	3.8
5	0	0	OFF	OFF	0	ON	OFF	4.4
5	0	5	OFF	ON	4.4	ON	OFF	4.4
5	5	0	ON	OFF	4.4	ON	OFF	4.4
5	5	5	ON	ON	4.4	ON	OFF	4.4

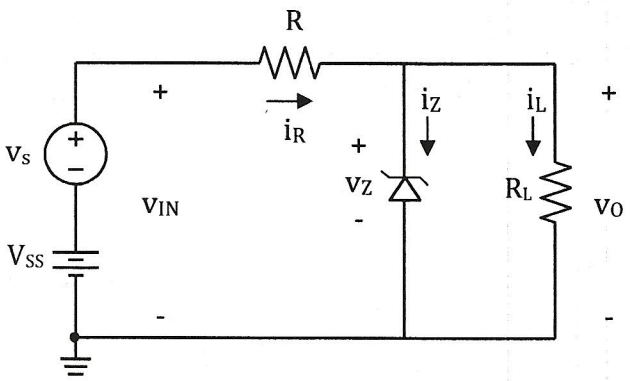
A	B	C	X	Y
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

$$X = B + C$$

$$Y = A + X = A + B + C$$

Q3. (20 pts)

a) Consider the zener voltage regulator circuit given below. The circuit parameters are listed on the right.



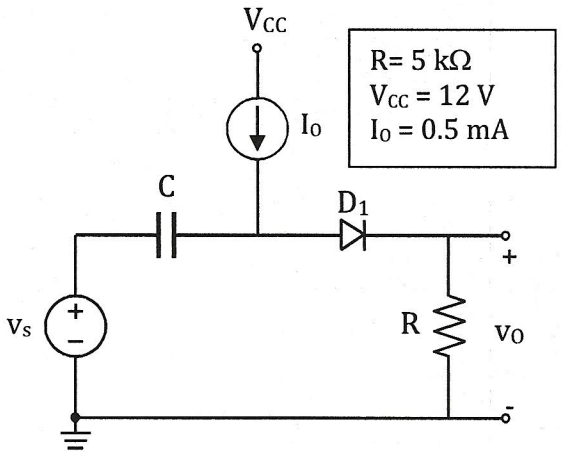
Circuit Parameters
V_{SS} = 8 volts
v_S = 0.5 sin $\omega_o t$ volts
R = 1 kΩ
R_L = 3 kΩ

Zener Diode
V_Z = 5 volts
r_Z = 15 Ω

i. Determine the DC component of the output voltage v_O.
ii. Determine the AC small signal component of the output voltage v_O.
iii. Calculate $V_{ripple\text{-}peak}/V_{DC}$ ratio at the input and output.
iv. Determine the range of RL over which the zener diode is always in the zener region.

b) Consider the circuit given below, with R= 5 kΩ, V_{CC} = 12 V. The input signal v_s (v_s = 25 sin $\omega_o t$ millivolts) is a small signal source. The capacitor C is assumed very large.
The diode is a pn-junction diode with turn-on voltage of V_γ=0.7 V.

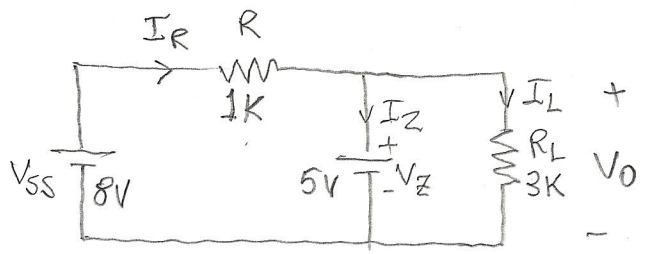
i. Draw the DC equivalent circuit and determine the DC component of the output voltage V_O.
ii. Draw the AC small signal equivalent circuit and determine the AC small signal component of the output.
iii. Determine the total voltage (DC+AC) at the output, v_O.
iv. Determine the limit on v_s for proper linear small signal modeling.



R= 5 kΩ
V_{CC} = 12 V
I_O = 0.5 mA

Q3.

a) i.



I. DC output voltage & currents

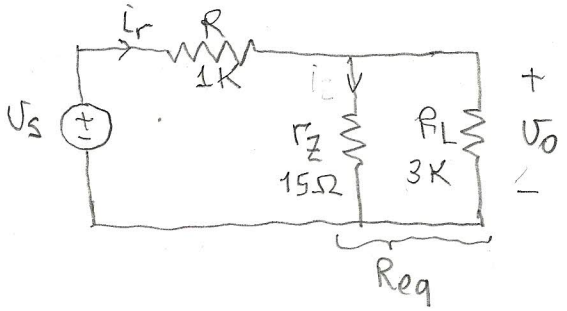
$V_O = V_Z = 5V$

$I_L = \frac{5V}{3K} = 1.33\ mA$

$I_R = \frac{8-5V}{1K} = 3\ mA$

$I_Z = I_R - I_L = 3 - 1.33 = 1.66\ mA$

ii. AC model:



$v_s = 0.5 \sin \omega t$ volt

$Req = 15\Omega // 3000\Omega \simeq 15\Omega$

$v_o = \frac{Req}{Req + R} v_s = \frac{15}{1000+15} v_s$

$\simeq \frac{15}{1015} . 0.5 \sin \omega t$ volt

$v_o = 0.45 \sin \omega t$ millivolt.

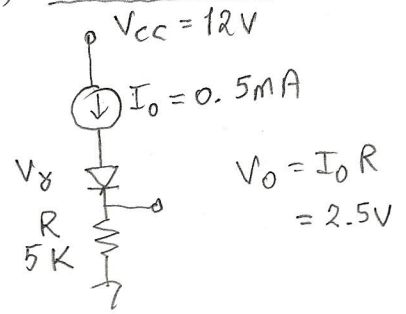
iii. $\frac{V_{ripple\text{-}peak}}{V_{DC}} \simeq \frac{0.45 \times 10^{-3}}{5V} = 0.15 \times 10^{-3} = 0.015\ \%$

iv. In the DC model, there should be zener current such that $I_Z > 0$.

$I_L = \frac{5}{R_L}$, $I_R = \frac{8-5V}{1K} = 3\ mA$

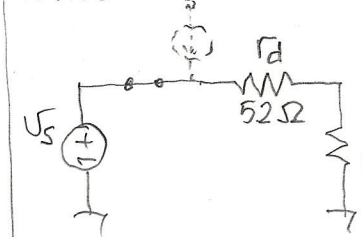
$I_Z = I_R - I_L = 3 - \frac{5}{R_L} > 0 \Rightarrow 3 > \frac{5}{R_L} \Rightarrow R_L > \frac{5}{3} = 1.66\ K$

(b) i. DC Model:



$V_O = I_O R = 2.5V$

ii. AC Model: $r_d = \frac{26mV}{I_D} = \frac{26mV}{0.5mA} = 52\Omega$



$v_o = \frac{R}{R + r_d} . v_s$

$= \frac{5000}{5052} v_s = 0.99 v_s$

$= 24.7 \sin \omega_o t$ mV

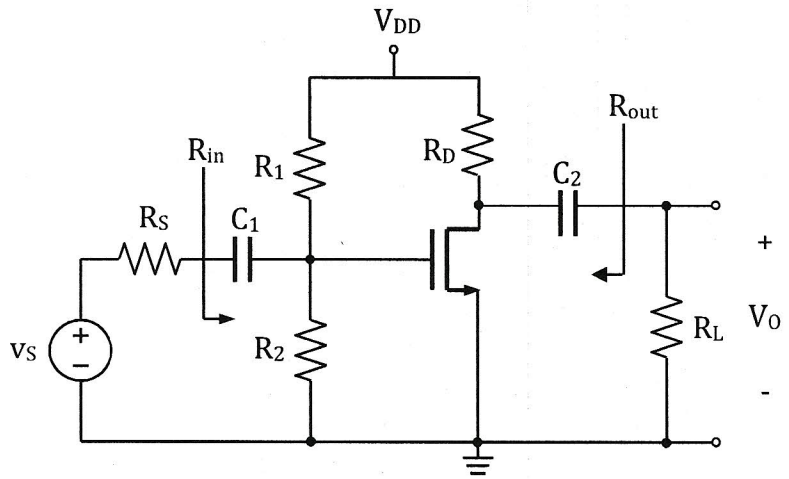
iii. $v_o = 2.5V + 24.7 \sin \omega_o t$ mV

iv. $v_d << 5.2$ mV (Small signal voltage over diode)

$v_d = \frac{r_d}{r_d + R} v_s = \frac{52}{5000+52} v_s << 52$ mV $\Rightarrow v_s << 5052$ mV

$v_s < 505.2$ mV

Q4. (20 pts) Consider the MOS amplifier given below. The input coupling capacitor C_1 and the load coupling capacitor C_2 are assumed very large.

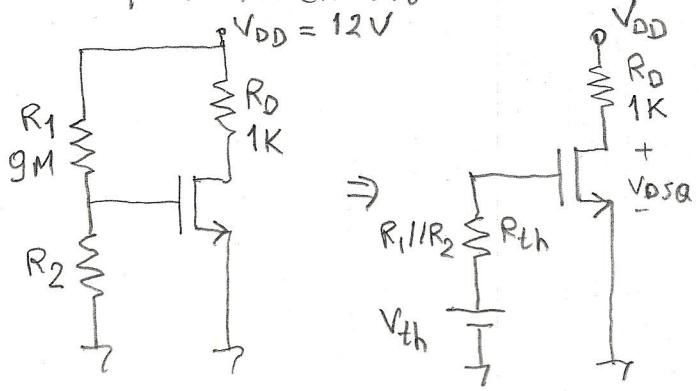


Circuit Parameters
$V_{DD} = 12$ V
$R_S = 1$ kΩ
$R_1 = 9$ MΩ
$R_D = 1$ KΩ
$R_L = 4$ KΩ

Transistor Parameters
$V_{Tn} = 1$ V
$K_n = 4$ mA/V²
$V_A = 100$ V

(a) Draw the DC equivalent circuit.
(b) Determine the values of R_2 so that $V_{GSQ} = 3$ V.
(c) Determine I_{DQ} and V_{DSQ} and also the state of the transistor.
(d) Find g_m and r_{ds}.
(e) Draw a complete AC small-signal equivalent circuit for the amplifier.
(f) Find the input resistance R_{in} and the output resistance R_{out}.
(g) Determine the voltage gain $A_v = v_o/v_s$.

(a) DC Equivalent circuit:



(b) $V_{GSQ} = 3V$

$$\frac{R_2}{R_1+R_2} \cdot V_{DD} = V_{th} = V_{GSQ}$$

$$\frac{R_2}{R_1+R_2} \cdot 12 = 3$$

$$\frac{R_2}{R_1+R_2} = \frac{3}{12} = \frac{1}{4}$$

$$4R_2 = R_1 + R_2 \Rightarrow R_2 = \frac{R_1}{3} = 3M$$

$$R_{th} = R_1 // R_2 = \frac{3 \cdot 9}{12} = 2.25\,M$$

(c) Assume SAT ($V_{DSQ} \geq V_{GSQ} - V_{Tn} = 3 - 1\,V = 2V$?)

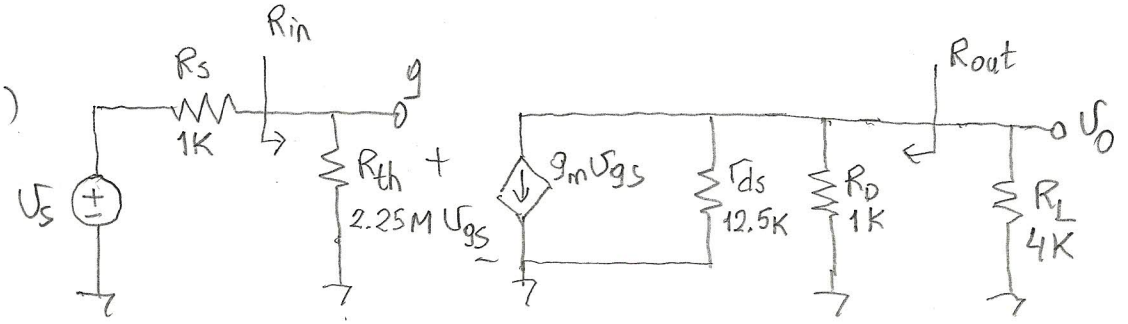
SAT current: $I_{DQ} = \frac{K_n}{2}(V_{GSQ} - V_{Tn})^2 = \frac{4\,mA/V^2}{2}(3-1\,V)^2 = 8\,mA$

$V_{DSQ} = V_{DD} - I_{DQ} R_D = 12 - (8\,mA)(1K) = 7V > 2V$ (SAT is OK.)

(d) $g_m = K_n(V_{GSQ} - V_{Tn}) = (4\,mA/V^2)(2V) = 8\,mA/V$

$$r_{ds} = \frac{V_A}{I_{DQ}} = \frac{100\,V}{8\,mA} = 12.5K$$

(e)



$R_{in} = R_{th} = 2.25\,M\Omega$

$R_{out} = r_{ds} // R_D = (12.5K) // (1K) = 0.89K$

(f) $A_v = \frac{R_{th}}{R_s + R_{th}} \cdot (-g_m) R_{eq}$ where $R_{eq} = r_{ds} // R_D // R_L$

$R_{eq} = \underbrace{12.5K // 1K}_{0.89K} // 4K = (0.89K) // 4K = 0.82K$

$A_v = \left(\frac{2250}{2250+1}\right)(-8\,mA/V)(0.82K) = -6.55$